REMARKS

Claims 1-7 and 9-16 are pending in this application, of which claims 7, 13, 15 and 16 have been amended. Claim 8 is canceled. No new claims have been added.

Claims 7 and 13 stand rejected under 35 U.S.C. § 101 for being directed to non-statutory subject matter.

Accordingly, claims 7, 13 and 15 have been amended to remove the noted limitations and to recite language which clarifies that the evaluation pattern has at least one defect of which transferability onto said transfer target (semiconductor wafer) has previously been evaluated. The "tangible result" for this apparatus (or method) is that the defect detected on the transfer target in the exposure area may be compared with the previously evaluated defect in the evaluation pattern to determine if the detected defect will actually be transferred.

Thus, the 35 U.S.C. § 101 rejection should be withdrawn.

Claims 1-16 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent Publication 2002/0194576 to Toyama (hereafter, "**Toyama**").

Applicant respectfully traverses this rejection.

Toyama discloses a method of evaluating the exposure property of data to wafer in which errors of the production of photomask and the formation of patterns caused by defocus in the transfer of data to wafer are considered. Accordingly, errors of the production of photomask and deformation of patterns caused by defocus can be evaluated in the stage of design data. Oversize processing and undersize processing are given to pattern data of the object of process by figure

operation for the whole pattern data within errors of the production of photomask according to the specification thereof, and simulation is used as a reference to original pattern data of the object of process, the oversize data in which oversize processing is given to the pattern data and the undersign data in which undersize processing is given to the pattern data, in which the wafer exposure simulation is carried out under the condition of zero focus, or under the each exposure condition of zero focus, a given value minus defocus or a given value plus defocus. The exposure property of data to wafer is evaluated from the results of the wafer exposure simulation.

None of the cited portions of the disclosure of **Toyama** discloses that at least one evaluation pattern is formed in an area different from said exposure area, as shown in FIG. 4A of the instant application. None of the drawings in **Toyama** shows anything other than the various ways a pattern formed on a semiconductor wafer may be different from design data as a result of the optical proximity effect.

Accordingly, claims 7, 13, 15 and 16 have been amended to clarify this feature, while claim 8 has been canceled.

Furthermore, it should be noted that a reticle of the present invention has a device pattern formed in an exposure area, and evaluation pattern(s) formed in an area different from the exposure area. That is, the present invention includes a device pattern and evaluation pattern(s) on one reticle.

This makes it possible to comparatively observe the detected defects in the exposure area of the reticle and evaluation pattern(s) under the same inspection wavelength, allows an exact

judgment on whether or not the detected defects adversely affect the transfer of the device pattern, and consequently allows an easy and exact judgment regarding the necessity of the correction of such defects.

On the other hand, **Toyama** relates to a proving and evaluation technique of the transfer property of design data to wafer by means of the technique of exposure simulation. **Toyama** discloses that a simulation is carried out only to the patterns transferred from design data. In **Toyama**, a mask is actually used for forming a simulation model. However, **Toyama** fails to disclose a reticle (mask) having both a device pattern and at least one evaluation pattern, as recited in claims 1, 7, 13 and 15, as amended.

Thus, the 35 U.S.C. § 102(e) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-7 and 9-16, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Petition for Extension of Time
Check in the amount of $120.00

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